Amendments to the Specification

Please replace the paragraph beginning at page 8, line 20, with the following rewritten paragraph:

-- Figure 4A is a schematic diagram of the MRAM memory cell array 200 illustrating a method for programming a unit cell 100' to store a logic value 0. The unit cell 100' is coupled to bitline B2 and wordline W2. As illustrated in Figure 4A, bitlines B1 and B3 are disposed adjacent to bitline B2, which is coupled to unit cell 100'. In addition, wordlines W1 and W3 are formed adjacent to wordline W2, which also is coupled to unit cell 100'. To program unit cell 100' to store a logic value 0, bit current 403 and bit current 402 are [[is]] placed on bitlines B1 and B3, respectively, in the directions shown in Figure 4A, which are opposite each other. In addition, word current 406 and word current 407 are [[is]] placed on wordlines W1 and W3, respectively, in the directions shown in Figure 4A, which are opposite each other. --

Please replace the paragraph beginning at page 9, line 6, with the following rewritten paragraph:

-- Figure 4B is a schematic diagram of the MRAM memory cell array 200 illustrating a method for programming the unit cell 100' to store a logic value 1. To program unit cell 100' to store a logic value 1, bit current 412 and bit current 411 are [[is]] placed on bitlines B1 and B3, respectively, in the directions shown in ~~Figure 4A~~ Figure 4B, which are opposite each other. In addition, word current 420 and word current 421 are [[is]] placed on wordlines W1 and W3 in the directions shown in ~~Figure 4A~~ Figure 4B, which are opposite each other. It should be noted that the current directions on the bitlines 202 and the wordlines 204 when programming a logic value 1 are the inverse of the current directions on the bitlines 202 and the wordlines 204 when programming a logic value 0. --